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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,563	02/16/2004	Yoshiro Iwasa	9319S-000666	9016

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,563	IWASA, YOSHIRO	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/779563 Attorney's Docket #: 9319S-00666
Filing Date: 2/16/2004; claimed foreign priority to 2/21/2003

Applicant: Iwasa

Examiner: Alexander Williams

Applicant's election of the species of figures 1-9 (claims 1 to 18) filed 7/29/05, has been acknowledged. However, there are only claims 1-6 exists.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claims 1 to 6 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 3, it is nuclear and confusing to what is meant by "a frame-shaped land;...first to fourth support portions formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and first to fourth groups of lead members having first ends and second ends, the first ends being fixed to the land, and the second ends being parallel in each group." Where are they is the drawing? What is the different form the lands and the lead members? Are they the same?

In claims 4 and 6, it is unclear and confusing to what is meant by "**fifth to eighth groups of wiring patterns** formed on the second surface of the substrate and having first ends and second ends, the first ends being connected to the first to fourth groups of wiring patterns, and the second ends being parallel in each group." Where fifth to eighth groups of wiring patterns in the drawing?

Any of claims 1 to 6 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 6, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Miyaki et al. (U.S. Patent # 6,340,837 B1).

1. Miyaki et al. (figures 1 to 23) specifically figures 1 to 3 show a lead frame for packaging **1** a semiconductor chip **10**, the lead frame comprising:

a frame-shaped land **2**;

a die pad **5** for mounting the semiconductor chip;

first to fourth support portions **3** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and
first to fourth groups of lead members **2** having first ends and second ends, the first ends being fixed to the land, and the second ends being parallel in each group.
2. A lead frame according to Claim 1, Miyaki et al. show wherein the first to fourth groups of lead members are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the land and the longer bases of which face sides of the land, and the second ends of the first to fourth groups of lead members are along the shorter bases of the first to fourth trapezoidal areas.
3. Miyaki et al. (figures 1 to 23) specifically figures 1 to 3 show a method for manufacturing a semiconductor device including a lead frame having a frame-shaped land **2**; a die pad **5** for mounting the semiconductor chip **10**; first to fourth support portions **3** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and first to fourth groups of lead members **2** having first ends and second ends, the first ends being fixed to the land, and the second ends being parallel in each group, the method comprising the steps of:
(a) cutting the first to fourth groups of lead members according to the size of the semiconductor chip to be packaged;
(b) mounting the semiconductor chip on the die pad;
(c) bonding the first to fourth groups of lead members and the semiconductor chip with a plurality of wires **12**;
(d) fitting terminals to the land, for connecting the first to fourth groups of lead members to an external circuit; and
(e) encapsulating **13** the lead frame and the semiconductor chip.
4. Miyaki et al. (figures 1 to 23) specifically figures 1 to 3 show a package **1** for packaging a semiconductor chip **10**, the package comprising:
a substrate **5** for mounting the semiconductor chip, the substrate having a first surface and a second surface;
first to fourth groups of terminals formed on the first surface of the substrate;
first to fourth groups of wiring patterns **2** formed on the substrate and connected to the first to fourth groups of terminals; and
fifth to eighth groups of wiring patterns **2** formed on the second surface of the substrate and having first ends and second ends, the first ends being connected to the first to fourth groups of wiring patterns, and the second ends being parallel in each group.

5. A package according to Claim 4, Miyaki et al. show wherein the fifth to eighth groups of wiring patterns are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the substrate and the longer bases of which face sides of the substrate, and the second ends of the fifth to eighth groups of wiring patterns are along the shorter bases of the first to fourth trapezoidal areas.
6. Miyaki et al. (figures 1 to 23) specifically figures 1 to 3 show a method for manufacturing a semiconductor device including a package **1** having a substrate **5** for mounting the semiconductor chip, the substrate having a first surface and a second surface; first to fourth groups of terminals formed on the first surface of the substrate; first to fourth groups of wiring patterns formed on the substrate and connected to the first to fourth groups of terminals; and fifth to eighth groups of wiring patterns formed on the second surface of the substrate and having first ends and second ends, the fast ends being connected to the first to fourth groups of wiring patterns, and the second ends being parallel in each group, the method comprising the steps of:
(a) cutting the fifth to eighth groups of wiring patterns according to the size of the semiconductor chip **10** to be packaged;
(b) mounting the semiconductor chip on the substrate;
{c} bonding the fifth to eighth groups of wiring patterns and the semiconductor chip with a plurality of wires **12**; and
(d) encapsulating **13** the second surface of the package and the semiconductor chip.

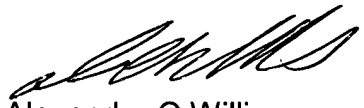
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/666,670,669,671,672,676,696,668	9/19/05
Other Documentation: foreign patents and literature in 257/666,670,669,671,672,676,696,668	9/19/05
Electronic data base(s): U.S. Patents EAST	9/19/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/19/05